CLAIMS:

1. Method of manufacturing a semiconductor device (10) in which a semiconductor body (1) of silicon is provided, at a surface thereof, with a semiconductor region (4) of a first conductivity type, in which region a second semiconductor region (2A,3A) of a second conductivity type, opposite to the first conductivity type, is formed forming a pn-junction with the first semiconductor region (4) by the introduction of dopant atoms of the second conductivity type into the semiconductor body (1), and wherein, before the introduction of said dopant atoms, an amorphous region is formed in the semiconductor body (1) by means of an amorphizing implantation of inert atoms, and wherein, after the amorphizing implantation, temporary dopant atoms are implanted in the semiconductor body (1), and wherein, after introduction of the dopant atoms of the second conductivity type, the semiconductor body is annealed by subjecting it to a heat treatment, characterized in that dopant atoms of the second conductivity type are introduced into the semiconductor body (1) by means of ion implantation, and the semiconductor body is annealed by a heat treatment at a temperature in the range of about 500 to about 800 degrees Celsius.

2. Method according to claim 1, characterized in that the semiconductor body (1) is annealed by a heat treatment at a temperature in the range of 550 to about 750 degrees Celsius.

3. Method according to claim 1 or 2, characterized in that the implantation of the temporary dopant atom is performed before the implantation of the dopant atoms of the second conductivity type, and between these implantations the semiconductor body (1) is annealed by a further heat treatment in the same temperature range as the other heat treatment.

4. Method according to claim 1, 2 or 3, wherein the semiconductor device is formed as a field effect transistor, in which method the semiconductor body (1) of silicon is provided, at the surface thereof, with a source region and a drain region (2,3) of the second conductivity type, which are both provided with extensions (2A,3A), and with a channel

region (4) of the first conductivity type between the source region and the drain region (2,3), and with a gate region (5) separated from the surface of the semiconductor body (1) by a gate dielectric (6) above the channel region (4), characterized in that first semiconductor region (4) is formed as a part of the channel region (4) and the source and drain extensions (2A,3A) are formed as a part of the second semiconductor region (2A,3A).

5. Method as claimed in any one of the preceding claims, characterized in that for the first conductivity type the n-conductivity type is chosen, for the dopant atoms of the second conductivity type Boron atoms are chosen and for the temporary dopant atoms Fluor atoms are chosen.

6. Method according to claim 3 or 4, characterized in that for the amorphizing implantation of inert ions, ions are chosen from a group comprising Ge, Si, Ar or Xe.

7. Method as claimed in any one of the preceding claims, characterized in that for the annealing heat treatments a time is chosen between 1 second and 10 minutes.

8. A semiconductor device (10) obtained with a method as claimed in any one of the preceding claims.

9. A semiconductor device (10) as claimed in claim 8, characterized in that the device comprises a field effect transistor.